IN THE CLAIMS

1. (Twice amended) A receiver circuit arranged in a receiving [A clock phase detecting circuit arranged in a receiving] unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a signal at a predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said signal identification clock to said identifying circuit;

an equalizing circuit for subjecting said signal obtained by demodulating the multilevel orthogonal modulated signal to an equalizing process; and

a clock phase detecting unit for detecting a phase component of said signal identification clock based on errors between input and output signals of said equalizing circuit and then for supplying said phase component to said clock regenerating circuit;

wherein said clock phase detecting unit includes:

an error detecting unit for detecting a signal error between said input and output signals of said equalizing circuit[:]; and

a clock phase calculating unit for detecting the phase component of said signal identification clock by calculating the detection outputs from said error detecting unit.

2. (Twice amended) A receiver circuit arranged in a receiving [A clock phase detecting circuit arranged in a receiving] unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a signal at a predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said

identifying circuit to supply said signal identification clock to said identifying circuit;

an equalizing circuit for subjecting said signal obtained by demodulating the multilevel orthogonal modulated signal to an equalizing process; and

a clock phase detecting unit for detecting a phase component of said signal identification clock based on input and output signals of said equalizing circuit and then for supplying said phase component to said clock regenerating circuit;

wherein said clock phase detecting unit comprising:

an error detecting unit for detecting a signal error between said input and output signals of said [equilizing] equalizing circuit;

a signal inclination detecting unit for detecting the inclination of said demodulated signal; and

a clock phase calculating unit for operating the phase component of said signal identification clock by calculating based on respective outputs from said error detecting unit and said signal inclination detecting unit.

3. (Amended) A receiver circuit arranged in a receiving [The clock phase detecting circuit arranged in the receiving] unit of multiplex radio equipment, according to claim 2, wherein said signal inclination detecting unit comprising:

a delaying unit for delaying the output from said identifying circuit; and

a comparing unit for comparing the output from said identifying circuit with the output from said delaying unit to detect the inclination of said demodulated signal.

4. (Amended) A receiver circuit arranged in a receiving [The clock phase detecting circuit arranged in the receiving] unit of multiplex radio equipment, according to claim 2, wherein said identifying circuit is operated with high speed clocks; and wherein said signal inclination detecting unit comprising:

a delaying unit for delaying the output from said identifying circuit, said delaying unit being operated with said high speed clocks;

a latching unit for holding the output from said identifying circuit and the output from said delaying unit with clocks slower than said high speed clocks; and

a comparing unit for comparing the output of said identifying circuit held in said latching unit with the output from said delaying unit to detect the inclination of said demodulated signal.

5. (Twice amended) A receiver circuit arranged in a receiving [The clock phase detecting circuit arranged in the receiving] unit of multiplex radio equipment, according to claim 2, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulated signal; and wherein said signal inclination detecting unit includes a comparing unit that compares outputs of said plural identifying units with each other to detect the inclination of the demodulated signal when clocks with different predetermined phase shift between said plural identifying units are supplied to said plural identifying units.

6. (Amended) A receiver circuit arranged in a receiving [The clock phase detecting circuit arranged in the receiving] unit of multiplex radio equipment, according to claim 2, wherein said clock phase calculating unit is formed as a multiplying unit that subjects the output

of said error detecting unit and the output of said signal inclination detecting unit to a multiplying calculating process.

7. (Amended) A receiver circuit arranged in a receiving [The clock phase detecting circuit arranged in the receiving] unit of multiplex radio equipment, according to claim 2, wherein said clock phase calculating unit is formed as an exclusive OR calculating unit that subjects the output of said error detecting unit and the output of said signal inclination detecting unit to an exclusive OR calculation process.

8. (Thrice amended) A receiver circuit arranged in a receiving [A clock phase detecting circuit arranged in a receiving] unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a signal at a predetermined identification level, said signal being obtained by demodulating a multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said signal identification clock to said identifying circuit;

an equalizing circuit for subjecting said signal obtained by demodulating the multilevel orthogonal modulated signal to an equalizing process; and

a clock phase detecting unit for detecting a phase component of said signal identification clock based on input and output signals of said equalizing circuit and then for supplying said phase component to said clock regenerating circuit;

wherein said clock phase detecting unit comprises:

an error detecting unit for detecting an input signal to output signal error of said [equilizing] equalizing circuit;

a signal inclination detecting unit for detecting the inclination of said demodulated signal;

a clock phase calculating unit for detecting the phase component of said signal identification clock by calculating based on the respective outputs from said error detecting unit and said signal inclination detecting unit;

a specific signal judging unit for judging whether a specific signal exists; and

a gating unit for [producting] producing the phase component of said signal identification clock obtained by said clock phase calculating unit when said specific signal judging unit judges that said specific signal exists.

9. (Amended) A receiver circuit arranged in a receiving [The clock phase detecting circuit arranged in the receiving] unit of multiplex radio equipment, according to claim 8, wherein said signal inclination detecting unit comprising:

a delaying unit for delaying the output from said identifying circuit; and

a comparing unit for comparing the output from said identifying circuit with the output from said delaying unit to detect the inclination of said demodulated signal.

10. (Amended) A receiver circuit arranged in a receiving [The clock phase detecting circuit arranged in the receiving] unit of multiplex radio equipment, according to claim 8, wherein said identifying circuit is operated with high speed clocks; and wherein said signal inclination detecting unit comprising:

a delaying unit for delaying the output from said identifying circuit, said delaying unit being operated with said high speed clocks;

a latching unit for holding the output from said identifying circuit and the output from

said delaying unit with clocks slower than said high speed clocks; and

a comparing unit for comparing the output of said identifying circuit held in said latching unit with the output from said delaying unit to detect the inclination of said demodulated signal.

11. (Amended) A receiver circuit arranged in a receiving [The clock phase detecting circuit arranged in the receiving] unit of multiplex radio equipment, according to claim 8, wherein said identifying circuit comprises plural identifying units corresponding to the number of plural demodulated signals obtained by demodulating said multilevel orthogonal modulation signal; and wherein said signal inclination detecting unit includes a comparing unit that compares outputs of said plural identifying units with each other to detect the inclination of the demodulated signal when clocks with different predetermined phase amount between said identifying units are supplied to said plural identifying units.

12. (Amended) A receiver circuit arranged in a receiving [The clock phase detecting circuit arranged in the receiving] unit of multiplex radio equipment, according to claim 8, wherein said clock phase calculating unit is formed as a multiplying unit that subjects the output of said error detecting unit and the output of said signal inclination detecting unit to a multiplying calculating process.

13. (Amended) A receiver circuit arranged in a receiving [The clock phase detecting circuit arranged in the receiving] unit of multiplex radio equipment, according to claim 8, wherein said clock phase calculating unit is formed as an exclusive OR calculating unit that subjects the output of said error detecting unit and the output of said signal inclination detecting

unit to an exclusive OR calculation process.

14. (Twice amended) A receiver circuit arranged in a receiving [The clock phase detecting circuit arranged in the receiving] unit of multiplex radio equipment, according to claim 8, wherein said specific signal judging unit includes plural signal judging units that judge plural kinds of specific signals, and further comprising a selecting unit arranged between said [specific signal judging unit] plural signal judging units and said [gate] gating unit, for selecting decision results from said plural signal judging units.

15. – 46. (canceled)

47. (new) A receiver circuit arranged in a receiving unit of multiplex radio equipment, comprising:

an identifying circuit for identifying a demodulated signal at a predetermined identification level, said demodulated signal being obtained by demodulating a multilevel orthogonal modulated signal;

a clock regenerating circuit for regenerating a signal identification clock for said identifying circuit to supply said signal identification clock to said identifying circuit; and

a clock phase detecting section for detecting a phase component of said signal identification clock, based on clock-phase-detecting composite input information including any one of (i) a combination of demodulated signal which is obtained by demodulating the multilevel orthogonal modulated signal and an equalized demodulated signal and (ii) a combination of clock phase difference information to be supplied to said identifying circuit and

signal error differential information obtained by said identifying circuit, and then supplying said phase component to said clock regenerating circuit,

said clock phase detecting section including

a difference detecting unit, responsive to the receipt of said composite input information, for detecting any one of (I) difference information between the demodulated signal and the equalized demodulated signal and (II) a combination of the clock phase difference information and the signal error differential information, and

a clock phase calculating unit for calculating said phase component of said signal identification clock based on the output from said difference detecting unit.